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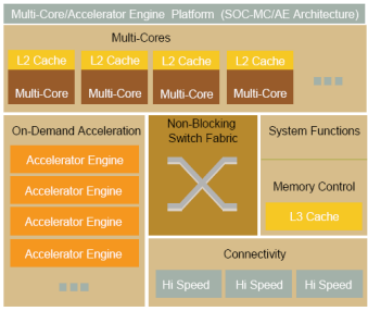
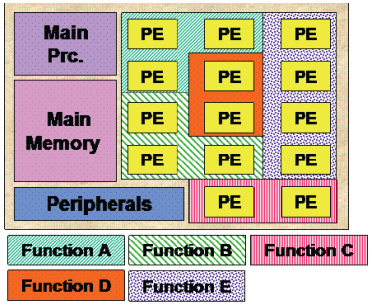
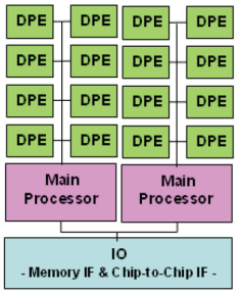
MPSoC IP Integration and Interoperability Challenges

Joachim Kunkel
VP&GM, Synopsys, Inc.
MPSoC 2008, Aachen

Summary

- MPSoCs are very application specific
  - Different architecture templates
- Next generation of MPSoCs will also have lots of processors and lots of non processor IP as well
- IP comes in many forms
  - Implementation
  - Verification
  - System-level
- Integration challenges at higher levels of abstraction tough
  - Interoperability and standards
  - Connected with the implementation flows
- SystemC TLM-2.0 is a great step forward
  - Will put increased focus on System-Level model availability

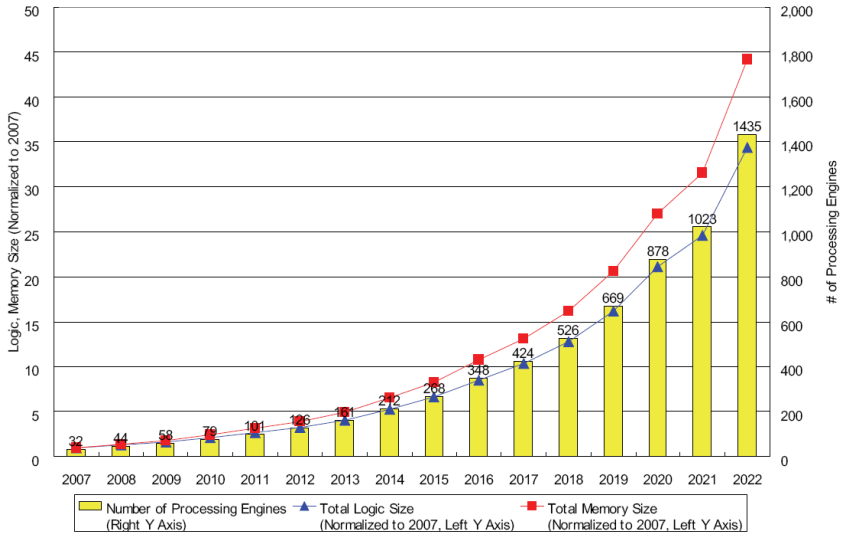
Where we seem to be going …

SoC		
Networking	Consumer Portable	Consumer Stationary
• Die area constant • # cores increases by 1.4× / year • Core frequency up by 1.05× / year • On-demand accelerator engine frequency up by 1.05× / year	• Rapid progress • Rapid increase in processing capability, constraints on power • Processing power increases by 1000× in the next ten years, • Lifecycles short.	• Performance > 120 TFlops in 2022 • Functions in software • Data Processing Engines • Worse performance–to-power ratio • Lifecycle long, application area wide
		

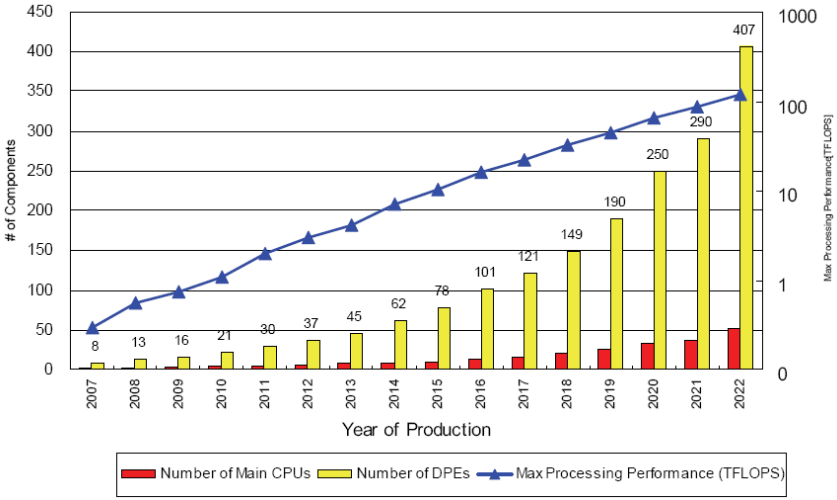
Source: ITRS 2007

Lot's of processors

Consumer Portable



Consumer Stationary

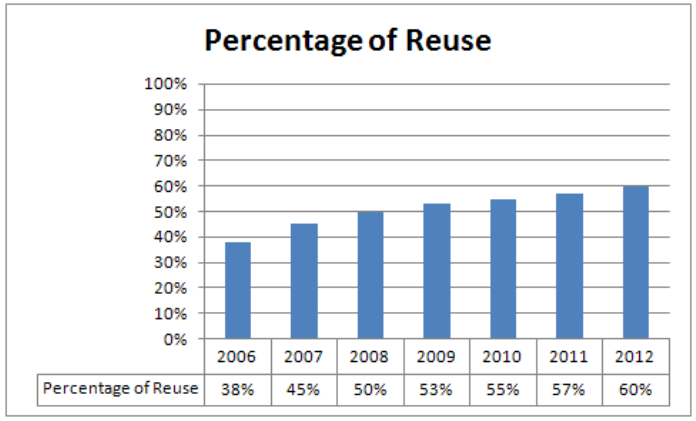


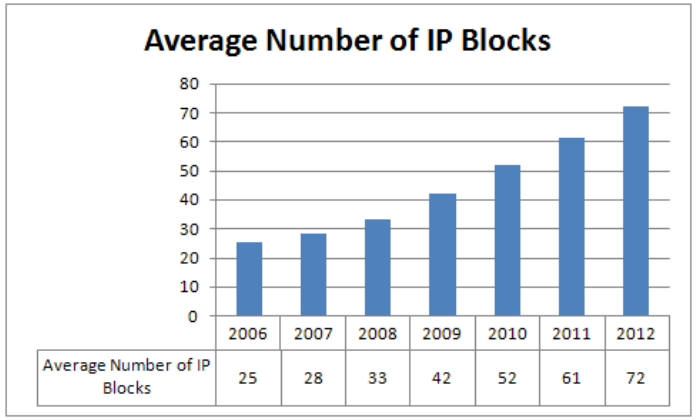
Source: ITRS 2007

But Software is not everything …

More IP Blocks, more Re-use

- Yes, there are lots of processors
- But there are other components too
- Especially the protocols in a design require lots of connectivity IP
- Mixed Signal content is also heavily growing
- So – let's not forget hardware IP

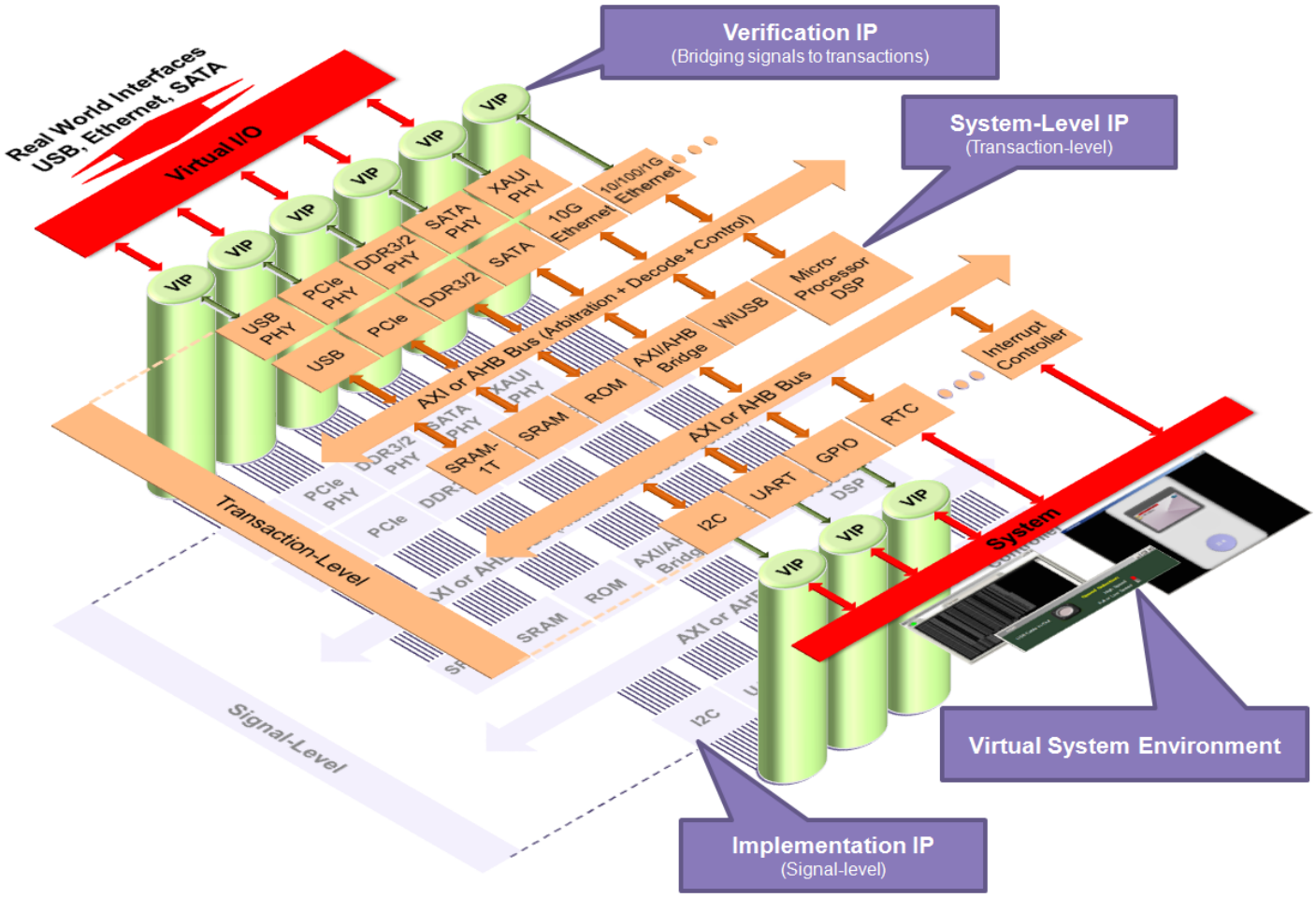




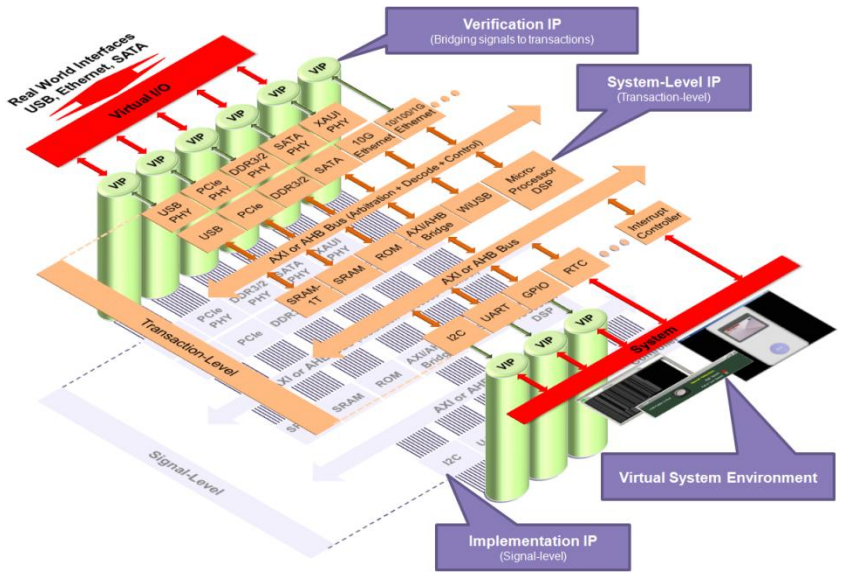
Source: Semico

IP Comes in Many Forms

Raising the Level(s) of Abstraction



System-Level Integration Challenges



- System model interoperability?
- How do users connect model abstractions
  - Transactor interoperability?
- How do users verify the TLM model(s) itself
  - TLM Assertions
  - Verification IP for TLM
  - Verify against what?
- How are models kept in sync
  - Against RTL
  - Against silicon revisions

➢ **System-level model interoperability and an integrated flow are required**

The Impact of SystemC TLM-2.0

Like Verilog in the 90's!

Bruegel, 1563
Tower of Babel

Hardware Description Languages		Virtual Platforms	
1980's	**1990's**	**1998 - 2008**	**Post 2008**
Age of Proprietary HDLs	**HDL Standardization**	**Proprietary APIs**	**Age of Interoperability**
Verilog VHDL HiLo DABL LASAR Aida M (Lsim) QuickSim UDL / I N dot, ISP, FBDL	Verilog VHDL HiLo DABL LASAR Aida M (Lsim) QuickSim UDL / I N dot, ISP, FPDL	Roll your own (C, C++) SystemC TLM-1.0 Synopsys Virtio ARM AXYS APIs CoWare N2C APIs Virtutech APIs VaST APIs …	TLM-2.0

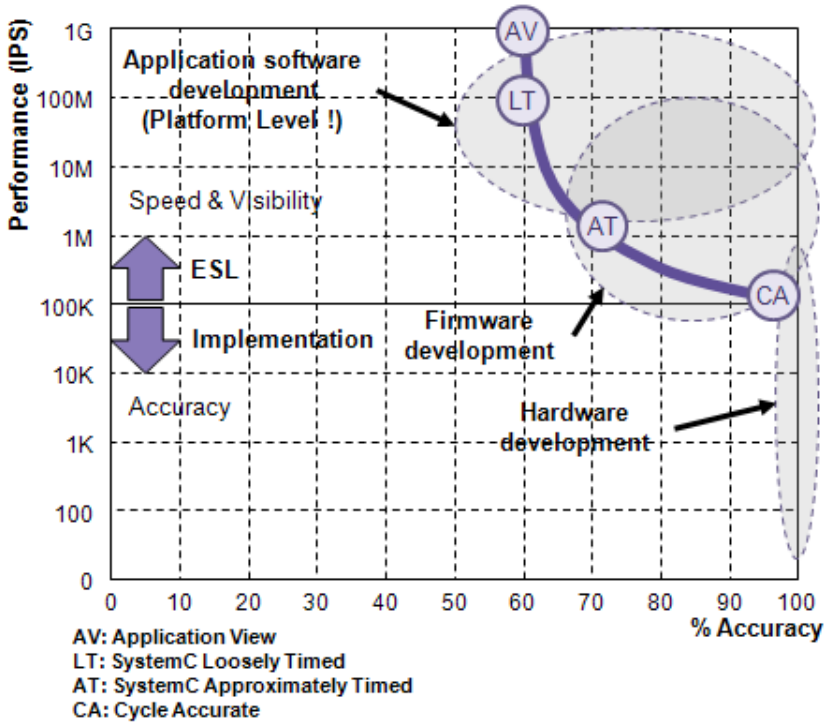
What it means for users:

1. Model interoperability
2. System-level simulation commoditization
3. **It's all about the models!**

The Impact of SystemC TLM-2.0
Enabling Interoperability and Scalability

- Previously proprietary (backdoor) APIs & new additions have now been standardized:

- (DMI) Direct Memory Interface
  - Direct backdoor access into memory
  - Allows un-inhibited ISS execution
- LT (Loosely Timed) modeling
  - Declare but don't execute timing
  - Allows speed/accuracy trade-offs
- Temporal Decoupling
  - Only synchronize when necessary
  - Allows multicore speedup



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